



IFW

PATENT
Customer No. 22,852
Attorney Docket No. 04329.3101-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Koji USUDA, et al.) **Prior** Group Art Unit: 2814
)
Div. of Application No.: 10/627,648, filed) **Prior** Examiner: Cao, Phat X.
July 28, 2003)
)
Filed: August 9, 2004)
)
For: SEMICONDUCTOR APPARATUS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicants bring to the attention of the Examiner the documents listed on the attached PTO-1449. Applicants are filing this Supplemental Information Disclosure Statement (IDS) before the mailing date of a first Office Action on the merits for the above-referenced application, to the undersigned representative's knowledge at the time this paper was filed. This IDS supplements the IDS filed on August 9, 2004.

Applicants attach copies of the listed documents. Applicants respectfully request that the Examiner consider the listed documents and indicate their consideration by making appropriate notation on the attached PTO-1449 Form.

In lieu of a statement of relevance or full translation of the non-English documents, Applicants enclose the attached Japanese Patent Office Action entitled "Notification of Reasons

for Rejection,” mailed July 20, 2004 in a counterpart foreign application, citing and setting forth the relevance of the attached documents. An English language translation of the Japanese Patent Office Action is also enclosed.

Applicants also attach a corrected copy of the PTO-1449 form filed with the IDS of August 9, 2004. This PTO-1449 corrects the prior application number listed on the form. Applicants respectfully request the Examiner initial and return a copy of this corrected PTO-1449 form.

This submission does not represent that a search has been made or that no better art exists, and does not constitute an admission that the listed documents are material or constitute “prior art.” If the Examiner applies the documents as prior art against any claim in the application and Applicants determine that the cited documents do not constitute “prior art” under United States law, Applicants reserve the right to present to the Office the relevant facts and law regarding the appropriate status of such documents.

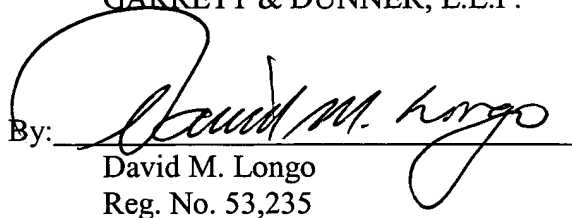
Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should the documents be applied against the claims of the present application.

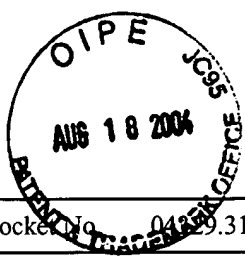
If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: August 18, 2004

By: 
David M. Longo
Reg. No. 53,235



INFORMATION DISCLOSURE CITATION

Atty. Docket No. 04929.3101-01	Div. of Appln. No. 1 0/627,648
Applicant Koji USUDA, et al.	
Filing Date August 9, 2004	Prior Group: 2814

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
2003-234472	08/2003	Japan			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce

Corrected form

OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3101-01	Div. of Appln. No.	1 0/627,648
Applicant	Koji USUDA, et al.		
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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	McKee et al. "PHYSICAL STRUCTURE AND INVERSION CHARGE AT A SEMICONDUCTOR INTERFACE WITH A CRYSTALLINE OXIDE", Science, Vol. 293, pages 468-471, (2001)
	Nishikawa et al., "DIRECT GROWTH OF SINGLE CRYSTALLINE CeO ₂ HIGH-K GATE DIELECTRICS", Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, pages 174-175, (2001)
	Gottschalk et al., "EPITAXIAL Pr ₂ O ₃ ON SILICON AS AN ALTERNATIVE GATE OXIDE FOR FUTURE CMOS APPLICATIONS", JOINT SESSION CRYSTALLINE OXIDES FOR GATE DIELECTRICS, Session N8.5/T6.5, pages 350-351, (2002)
	Tezuka et al., "NOVEL FULLY-DEPLETED SiGe-ON-INSULATOR pMOSFETs WITH HIGH-MOBILITY SiGe SURFACE CHANNELS", IEDM Tech. Dig., 946, IEEE, (2001)
	Welser et al.; "STRAIN DEPENDENCE OF THE PERFORMANCE ENHANCEMENT IN STRAINED-Si n-MOSFETs", IEDM, pages, 373-376, IEEE, (1994)
	Hirose et al.; "FUNDAMENTAL LIMIT OF GATE OXIDE THICKNESS SCALING IN ADVANCED MOSFETs", Semicond. Sci. Technol. Vol. 15, pages 485-490, (2000)

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce

The PTO did not receive the following listed item(s) NPL documents.